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EXAMINER	
VU, TUAN A	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/898,351	SUBRAHMANYAM ET AL.
	Examiner	Art Unit
	Tuan A Vu	2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed July 03, 2001.

Claims 1-20 have been submitted for examination.

Abstract

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

As per the instant abstract, the allowed maximum length of 150 words has been exceeded. Correction is required.

Specification

3. The disclosure is objected to because of the following informalities: the statement 'Backpatching in both the process ... is avoided' (pg. 12, line 13-15) is not constructed with correct standard English and appears like a segment of an unfinished sentence.

4. The disclosed element 'step 82(FIG. 4)' is not shown to be in the drawing Fig. 4 as indicated.

5. The disclosed element 'code cache 22' (pg. 12, line 9) should be 'code cache 27' instead.

Appropriate correction is required.

Drawings

6. The drawings are objected to because the legend 'STEP 82(FIG. 4)' in block 99 of Figure 6 is not found in Fig. 4 as indicated and this is also specified as one of the informalities in the specification.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action.

The objection to the drawings will not be held in abeyance.

Claim Objections

7. Claims 8 and 11 are objected to because of the following informalities:

As per claim 8, there is a '.." at the end of the claim whereas there should be only one period.

As per claim 11, there should be a description of what is contained in the computer readable medium, as recited in line 1, for performing 'analyzing a computer program...', e.g. containing a software product/program logic or instructions. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. Claims 13, 14 recite the limitation "said storage logic" in line 3, line 7 of claims, respectively. There is insufficient antecedent basis for this limitation in the claim. Examiner will regard this element as if it was a storage logic for storing counting logic (as inferred from claim 11, line 5) or alternatively any storage means as found in a given prior art.

b. Claims 1, 4, 16, 18, 19 recite the element 'said plurality of counters' (cl. 1, li 6; cl. 4, li. 3, cl. 16, li. 5,7; cl. 18, li. 1; cl. 19, li. 2-3). There is no antecedent basis for this limitation and it will be treated as a counter.

c. Claims 8, 9, 13, 14 recite 'said plurality of counting means' (cl. 8, li. 2; cl. 9, li. 3) and 'said plurality of counting logic' (cl. 13, li. 2; cl. 14, li. 3). There is no antecedent basis for this limitation and these elements will be treated alternatively as a counter, a counting means or a counting logic.

d. Claim 5 recites 'said code cache' (line 2); there is no antecedent basis for this and it will be treated as if it were counter cache.

e. Claim 11 recites logic for storing said counting logic of said plurality of blocks of code (line 7); this limitation is not clear as to how it would distinguish from a previous limitation as recited on line 5; hence is open to interpretation that it is either the same limitation or a broader limitation to that recited in line 5.

10. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

11. Claims 2-5, 12-15, and 17-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The elements recited as

'...said counter cache is full' (claim 2, claim 17) and

'... said most recently executed storing logic is full' (claim 12), the element 'storing logic' being interpreted as 'logic for storing said counting logic of said plurality ... most recently executed'(as inferred from claim 11, line 5),

are not supported by any explicit description in the specification.

The specification makes it clear in Fig. 4 via pg. 11-12, and Fig. 8 via pg. 15-16, that it is code cache 27(Fig. 3-4) that is determined to be full. Code cache (*code cache 27*) and *counter cache 25* as exhibited in Fig. 1 and 3, are two different entities, hence code cache is perceived as being distinct from elements 'counter cache' or 'logic for storing counting logic ... most recently executed' as claimed. From interpreting the claims in light of the specification, it is becoming evident that these elements should correspond to a counter cache being full; and there is no description of this in the specification. Hence, as provided, the specification and drawing were not described in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The

interpretation will be at best based on the understanding derived from the specification, i.e. one alternative way of interpreting being to equate *counter cache* to *code cache*, even though other ways of interpreting are possible.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> Note: 35 U.S.C. § 102(e), as revised by the AIPA and H.R. 2215, applies to all qualifying references, except when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. For such patents, the prior art date is determined under 35 U.S.C. § 102(e) as it existed prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. § 102(e)).

13. Claim 11 is rejected under 35 U.S.C. 102(e) as being anticipated by Holmberg et al., USPubN: 2001/0021959 (hereinafter Holmberg).

As per claim 11, Holmberg discloses a computer readable medium embodying program instructions for analyzing a computer program that includes a plurality of blocks of code (pg. 3, para 0028), comprising:

logic for executing said computer program (pg. 3 para 0028; pg. 5, para 0050);

logic for counting each time one of said blocks of code is executed (e.g. *access counter 25* -pg. 3 para 0034; *single basic block* - pg. 2, para 0013);

logic for storing the counting logic of said plurality of blocks of code (e.g. *reference number 23, counter 25* – Fig. 1a); and

logic for storing counting logic associated with plurality of blocks of code (e.g. *reference number 23, counter 25* – Fig. 1a).

But Holmberg does not explicitly disclose that the storing of counting logic of the plurality of blocks of code is for storing blocks that are most recently executed. Holmberg teaches placing in cache frequently used entities or blocks of code (e.g. pg. 3, para 0028; pg. 5, para 0054), hence has disclosed storing counter of blocks that are most recently executed.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holmberg et al., USPubN: 2001/0021959.

As per claim 12, official notice is taken that the memory space reclamation/replacement technique, e.g. LRU replacement algorithm, applied to cache when it is determined that cache capacity is towards being all used up was a well known concept at the time the invention was made. Even though Holmberg does not explicitly disclose determining when a counter cache is full, in view of the teachings by Holmberg to manage the memory with respect to size and exceptions implementation in regard to size violations (pg. 7, para 0067-0072), it would have been obvious for one of ordinary skill in the art at the time the invention was made to add the

limitation of determining when the cache is full as well known in the art and implement that to Holmberg's size allocation so to help anticipating resources exhaustion and rectify the contents of the cache in a timely fashion to avert memory crash.

16. Claims 1-10, and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holmberg et al., USPubN: 2001/0021959, in view of Burton et al., USPN: 6,738,865 (hereinafter Burton).

As per claim 1, Holmberg discloses a method to analyze a computer program that includes a plurality of blocks of code (pg. 3, para 0028), the method comprising:

executing said computer program (e.g. pg. 3 para 0028, pg. 5, para 0050);

using a counter for tracking each time one of said plurality of blocks is executed (e.g. *access counter 25* -pg. 3 para 0034; *single basic block* - pg. 2, para 0013);

maintaining a counter associated with a cache for storing said plurality of count references in a cache of said blocks of code that are most recently executed (e.g. *reference number 23, counter 25* – Fig. 1a).

But Holmberg does not disclose maintaining a counter cache for storing the counter of the plurality of blocks of code that are most recently executed. Nor does Holmberg disclose maintaining a storage area for storing counters associated with blocks of code that are not most recently executed. Holmberg teaches placing in cache frequently used data (e.g. pg. 5, para 0054), hence has disclosed storing in cache corresponding counter of blocks that are most recently executed. Further, organizing cache for code for execution so that only most executed code is cached and that the least recently used cache entries are replaced using some algorithm, e.g. LRU replacement, was known concepts by the time the invention was made. Burton, in a

method to maintain cache for execution involving memory access operations using counter analogous to Holmberg's approach, discloses a counter placed in cache for effecting listing of cache data according to the most frequently used priority manner, i.e. a counter cache to associate cache entries being ordered by the most recently accessed rank (e.g. Fig. 1-2). It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the counter means by Holmberg to implement the counter by Burton so that the cache now stores the counter for tracking the frequency of data access or execution, hence would expedite the process of replacing least frequently used versus most frequently used data in the cache.

Further, Burton discloses a storage area to store entries that have been demoted from the replacement in the cache based on the counter association with the priority given to most frequently accessed entries (*storage 6* – col. 4, lines 6-34 - Fig. 3), while Holmberg implements 2 memories to support each other in optimizing cache loading with support of counters (MM, SC, Fig. 1a-b). It would have been obvious for one of ordinary skill in the art at the time the invention was made to use Burton's approach of maintaining the demoted blocks in a storage area and add this to the maintaining of counter in the first cache as set forth above by Holmberg/Burton so that counters in data in the first cache (those cache blocks/entries that are not recently executed) can be demoted to be stored in the second memory as suggested by Holmberg, accomplishing thereby dynamically the cache replacement scheme while preserving the least recently accessed blocks for future reference, i.e. a concept known in the art of cache temporal and spatial replacement.

As per claim 2, official notice is taken that the replacement technique, e.g. LRU replacement algorithm, applied to cache when it is determined that cache capacity is nearly exhausted was a well known concept at the time the invention was made. Even though Holmberg does not explicitly disclose determining when a counter cache is full, in view of the teachings by Holmberg and Burton to manage the cache, it would have been obvious for one of ordinary skill in the art at the time the invention was made to add the limitation of determining when the cache is full as well known in the art and implement that to Holmberg/Burton's combination so to help anticipating resources exhaustion and rectify the contents of the cache in a timely fashion to avert memory crash.

As per claim 3, in view of the techniques taught by Burton and the rationale in claim 2, the limitation of copying blocks from cache to a storage area would also be obvious for the same rationale as set forth in claim 2.

As per claim 4, Holmberg teaches maintaining in cache the most frequently executed data (pg. 5, para 0050) and Burton teaches cache recording of LRU(least recently used) information (Fig. 2) in conjunction with demoting cache entries so they are stored into secondary area (re claim 1). Even though there is no explicit teaching by Holmberg on determining which count of block stored in cache has been least recently executed or on copying block into another storage when the cache is full, it would have been obvious for one of ordinary skill in the art at the time the invention was made to add this determining step based on the teachings by Burton to Holmberg's cache maintenance method because the use of a second storage area as suggested by Holmberg can be use to support the LRU policy as suggested by

Burton, i.e. to support the well-known case when cache limit has been reached, i.e. cache is full, as mentioned in claim 2 above.

As per claim 5, Holmberg does not explicitly teach checking counter cache to determine if a block is being executed other than a first time; and loading a counter associated therewith into the counter cache; but the concept to keep cache based on spatial and temporal proximity was a known concept at the time the invention was made. In view of Burton's teaching to associate a counter with a cache entry in order to determine its state over time (e.g. col 3, line 30 to col. 4, line 5), the limitation as to find out if a block is being executed other than a first time and to keep a count associated with such determination is implicitly disclosed. Hence, it would have been obvious for one of ordinary skill in the art at the time the invention was made to provide the counter cache as taught by Burton to Holmberg's most executed block cache maintenance policy because of the same rationale as mentioned in claim 1 and because a counter with a time tracking as taught by Burton would enhance the determination in the least temporally accessed data so well-known in the art of cache replacement.

As per claim 6, this claim is a system claim corresponding to the method of claim 1 and includes means to perform the same step limitations as mentioned therein; hence is rejected with the corresponding rejections as set forth therein.

As per claim 7, refer to claim 2 for rejection.

As per claim 8, Holmberg does not disclose means for copying one or more of the counters of the plurality of blocks from the counter cache to a storage area when the cache is full. But this limitation is similar to that of claim 3, and is rejected using the rationale as set forth therein.

As per claims 9 and 10, these claims correspond to claims 4 and 5, respectively, hence are rejected using the rationale as set forth therein.

As per claim 13, with reference to claim 12, Holmberg does not teach copying of counter logic of the most recently executed storing logic to a storage logic when said most recently logic is full. But suggests provision of size conflicts (pg. 7, para 0067-0072) when loading program data into memory and 2 memories to support each other in optimizing cache loading with support of counters (MM, SC, Fig. 1a-b). The notion of replacing least frequently used data in cache or fast memory when storage capacity thereof is near its limits was a known concept in the art of memory management at the time the invention was made. Referring to the teaching by Burton as set forth in claim 1, i.e. the use of a secondary storage to store entries that have been demoted from the replacement in the cache based on the cache-stored counter associated (e.g. Fig. 1-2) with the priority given to most frequently accessed entries (*storage 6* – col. 4, lines 6-34 - Fig. 3), it would have been obvious for one of ordinary skill in the art at the time the invention was made to implement Holmberg's method of managing the 2 fast memories so to apply the well-known concept of full cache replacement techniques along with the teachings by Burton for the same benefits and motivation as set forth in claim 1 and 2 above.

As per claim 14, this claim corresponds to claim 4 and include the same limitations therein such to determine the least recently used (LRU) blocks and their counter and copying these LRU blocks to another storage area when the cache or most recently used storing logic is full; hence is rejected with the rationale as set forth therein.

As per claim 15, refer to claim 5 for corresponding rejection.

As per claim 16, Holmberg discloses a system for analyzing analyze a computer program that includes a plurality of blocks of code (pg. 3, para 0028), the method comprising:

a counter for tracking each time one of said plurality of blocks is executed (e.g. *access counter 25* -pg. 3 para 0034; *single basic block* - pg. 2, para 0013);

maintaining a counter associated with a cache for storing said plurality of count references in a cache of said blocks of code that are most recently executed (e.g. *reference number 23, counter 25* – Fig. 1a).

But Holmberg does not disclose maintaining a counter cache for storing the counter of the plurality of blocks of code that are most recently executed. Nor does Holmberg disclose maintaining a storage area for storing counters associated with blocks of code that are not most recently executed. But these limitations have been addressed in claim 1 above and are rejected herein using the corresponding rationale as set forth therein.

As per claims 17-20, these claims correspond to claims 2-5, respectively, hence are rejected using the rationale as set forth therein.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for formal communications intended for entry)

or: (703) 746-8734 (for informal or draft communications, please consult Examiner before using this number)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA. , 22202. 4th Floor(Receptionist).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAT
June 10, 2004

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